

## Low Noise, Further Gained Power From GaAs E-pHEMT Amplifier

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### Abstract.

In first stage of each microwave receiver there is Low Noise Amplifier (LNA) circuit, and this stage has important rule in minimizing the system noise figure, provide enough gain with sufficient linearity, and assure a stable  $50 \Omega$  input impedance at a low power consumption. The design of a LNA in Radio Frequency/Microwave (RF/MW) circuit requires the trade-off many importance characteristics such as gain, Noise Figure (NF), stability, power consumption and complexity. This situation Forces the designers to make choices in the design of RF circuits.

In this paper the aim is to design and simulate a LNA circuit with high gain and low noise using E-pHEMT MGA-665P8 transistor for frequency of 4 GHz. The amplifier is manually designed using conventional technique, Smith chart was used to do a matching of the input and output of the amplifier. The matching network was designed with microstrip lines and it's single-stub with minimum lengths. A completed design of amplifier was optimized using Hewlett- Packard Advanced Design System (HP-ADS) software. A single stage LNA has successfully designed with 21.032 dB forward gain and 0.697 dB noise figure and working stably in the desired frequency.

### 1. Introduction

To amplify the received signal in a microwave system, a low noise amplifier (LNA) is required. Because any noise injected by components in a system is amplified by later gain stages along with the signal, it is essential that the signal be amplified early in the receiver chain while adding as little noise as possible. The goal of this paper is to design an LNA with lowest noise figure possible, with gain as high as possible for the given FET and information.

The operating frequency of the design is 4 GHz. Substrate used is Duroid RO3006 with  $\mu_r = 6.15$ , substrate thickness  $h = 25$  mils, and metallization thickness  $t = 0.5$  mils. The design utilizes one high-performance low noise GaAs FET transistor MGA-665P8 manufactured by Avago Technologies.

The design includes matching network with microstrip lines and standard lumped elements ( $R$ ,  $L$ ,  $C$ ) for the bias network. The matching network is single-stub with minimum lengths. The design is simulated and optimized in ADS, the Advance Design System by Agilent Technologies.

### 2. Analytical Analysis of the LNA

#### 2.1 Calculation of $\Gamma_s$ and $\Gamma_L$

From the S2P data provided by Avago Technologies [3], S-parameters at 4 GHz are obtained as follows.

**Table 1.** MGA-665P8 typical scattering parameters at  $f= 4GHz$ ,  $ZO = 50 \Omega$ ,  $VDS = 3 V$ ,  $ID = 20.5 mA$

Parameter	Mag	Ang
$S_{11}$	0.312	-95.5
$S_{12}$	0.007	74.6
$S_{21}$	6.369	-170.1
$S_{22}$	0.094	-74.7

The stability calculations below show that this transistor is unconditionally stable since  $k > 1$  and  $|\Delta| < 1$ .

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.045 \angle 122.2^\circ \therefore |\Delta| = 0.045, \quad < 1 \text{ and } |\Delta|^2 = 0.002$$

$$\begin{aligned} \therefore K &= \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} = \frac{0.897}{0.089} \\ &= 10.07 = 10.1, > 1 \end{aligned}$$

The noise figure data is provided as follows.

$$F_{min}(4.0\text{GHz}) = 1.45 \text{ dB}$$

$$\Gamma_{opt} = 0.37 \angle 88.6^\circ$$

$$r_n = R_n / 50 = 0.2 \text{ Ohms, since } R_n = 10.0 \text{ Ohms}$$

The value of  $F_{min}$  (Minimum Noise Figure) is taken to be one at 4.0 GHz since it's the closest value available from the data of the transistor. Then the noise figure parameter at this frequency is calculated as follows.

$$N_i = \frac{Z_o(F - F_{min})|1 + \Gamma_{OPT}|^2}{4R_n} = 0.272$$

In order to obtain minimum noise figure, the reflection coefficient  $\Gamma_S$  look into the source is matched to  $\Gamma_{opt}$ .

$$\Gamma_S = \Gamma_{OPT}^* = 0.37 \angle -88.6^\circ$$

With  $\Gamma_{IN}$  is set to be the conjugate of  $\Gamma_S$  the reflection coefficient looking into the load is shown below.

$$\Gamma_L = S_{22} + \frac{S_{12}S_{21}\Gamma_{OPT}}{1 - S_{11}\Gamma_{OPT}} = 0.0576 \angle -57.8^\circ$$

Therefore the transducer power gain is equal to the available power gain and its value is calculated to be,

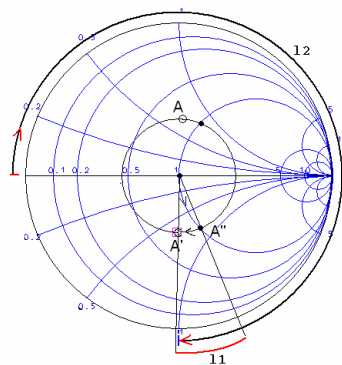
$$G_{Tmax} = \frac{|S_{21}|}{|S_{12}|} = (K - \sqrt{K^2 - 1}) = 16.5 \text{ dB}$$

This is a reasonable high gain. As a conclusion, with minimum noise level achieved at the input, the transistor can still produce high gain at the operating frequency.

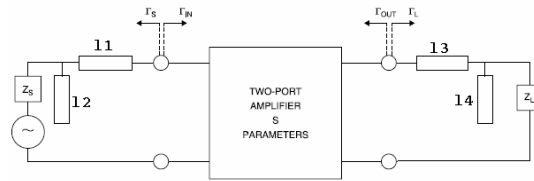
## 2.2 Design of the Matching network using Smith Chart

The position of  $\Gamma_S$  is located as point A in the Smith chart as shown in Fig.1. It is then transformed into admittance coefficient represented by point A'. It is desired to match point A' to the origin of the Smith chart, which represents the 50 Ohm transmission line. As the VSWR circle is drawn from point A', it intersect the  $T=1$  circle at 2 points which gives 2 solutions to the matching network. However, the point A'' is preferred because it allows total length of the input matching network to be shortest. Thus length  $l_1$  is read from the chart to be  $0.0328\lambda$  which is a series stub, and length  $l_2$  is  $0.3922\lambda$  which is an open-circuit stub.

Similarly, the output matching network is designed starting with the position of  $\Gamma_L$  on the Smith chart. With series stub length  $l_3$  is  $0.05\lambda$  and open-circuit stub length  $l_4$  is  $0.0149\lambda$ . The complete matching network schematic is shown in Fig.2. The physical dimensions of these microstrip lines are calculated with LineCalc tool available from ADS [4], based on the properties of the substrate used and the operating frequency, where the substrate used is Duroid RO-3006 with  $\epsilon_r=6.15$  substrate thickness  $h=25$  mil,  $\tan D=0.001$  and metallization thickness  $t=0.5$  mil. All the lines have 50 Ohm characteristic impedance, thus each has a width of 36.155 mils. The physical lengths of  $l_1$ ,  $l_2$ ,  $l_3$ , and  $l_4$  are 42.697 mils, 525.35 mils, 378.709 mils, and 26.736 mils respectively.



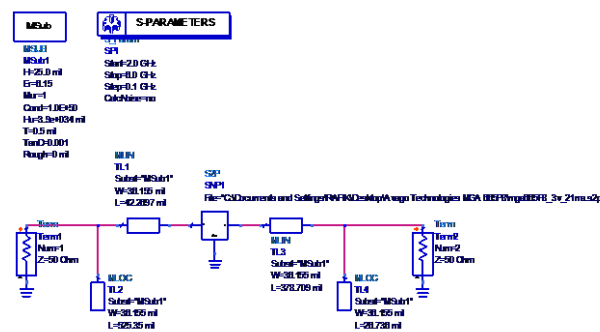
**Fig. 1.** Matching design of  $T_s$  to 50 Ohm line



**Fig. 2.** Schematic of the complete input and output matching network.

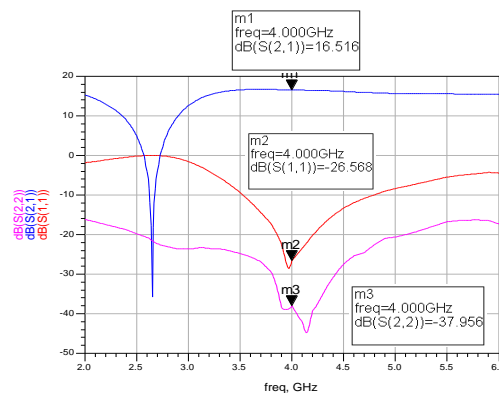
### 2.3 Biasing and ADS Simulations

The calculations performed in the previous sections are checked with ADS based on the S2P data. The ADS schematic is shown in Fig.3 below.



**Fig. 3.** ADS simulation with S2P data of the initial design.

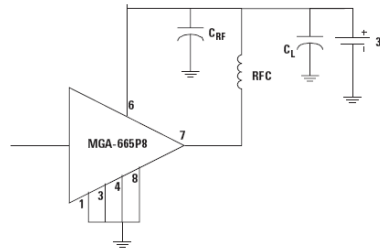
The results of  $S_{11}$  and  $S_{21}$  are plotted in Fig.4. Marker m1 shows the gain to be 16.410 dB agrees well with what was calculated.  $S_{11}$  and  $S_{22}$  show good match at input and output terminal.



**Fig. 4.** S-parameters of S2P simulation.

The MGA-665P8 has a single supply voltage whose maximum allowed value is 6V. The MGA-665P8 consists of two stages of amplifiers and requires the bias current to be supplied to both stages. The supply current to first and second stages is delivered through pin 6 and pin 7 respectively. An inductor serving as a

RFC needs to be inserted between the supply and pin 7. Based on the data provided by Avago Technologies, a bias network is designed to bias the transistor at  $V_d = 3V$ ,  $I_d = 20.5mA$ . A schematic of this bias network [5] incorporated into the matching network is shown in Fig. 5. The new gain obtained in this circuit is slightly higher from the circuit simulated with S2P block. The biasing is tuned with different drain voltages to obtain minimum noise figure and the data is reported in Table 2.



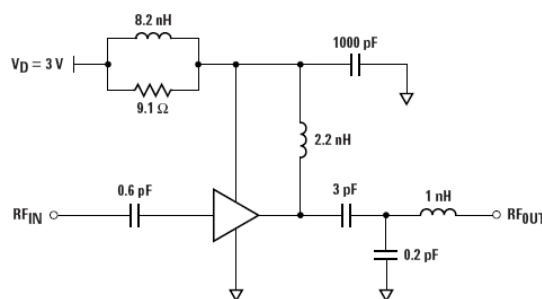
**Fig. 5.** Biasing scheme for MGA-665P8 [3].

**Table 2.** Tuning of  $V_d$  for noise figure values

$V_d$ (V)	$NF_{min}$ (dB)	NF (dB)	Gain (dB)
2	0.908	1.004	13.003
3	0.779	0.890	17.083
4	0.717	0.839	19.895
5	0.682	0.810	22.044
6	0.658	0.792	23.781

The data shows that minimum noise figure and noise figure at terminal can be reduced if applied higher drain voltage, however the difference is small and biasing at 4V leaves the transistor good protection over voltage variation. At 4.5V, the gain is also improved from that obtained in bias network at  $V_d = 3V$ . The plot in Fig. 8 shows the minimum noise figure and noise figure with  $V_d = 4.5V$ . The plot in Fig. 10 shows the gain ( $S_{21}$ ) and  $S_{11}$  values at 4.5 drain voltages. The values of  $S_{21}$  and  $S_{11}$  at 4 GHz for  $V_d = 4.5V$  are 21.032 dB and - 32.847 dB respectively.

The layout of the amplifier was done using the layout conversion tool of ADS and it is as shown in fig. 11.



**Fig. 6.** Basic DC biasing network [3].

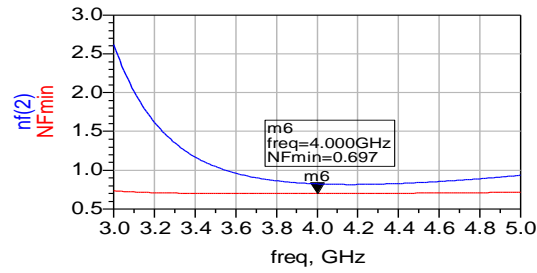


Fig. 7. Complete schematic of optimized low noise amplifier design with matching network.

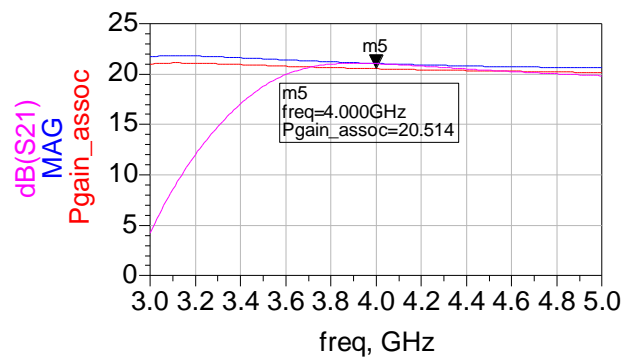


Fig. 8. Plot of minimum noise figure ( $NF_{min}$ ) and noise figure ( $nf(2)$ ) both in dB for LNA with bias of  $V_d = 4.5V$ .

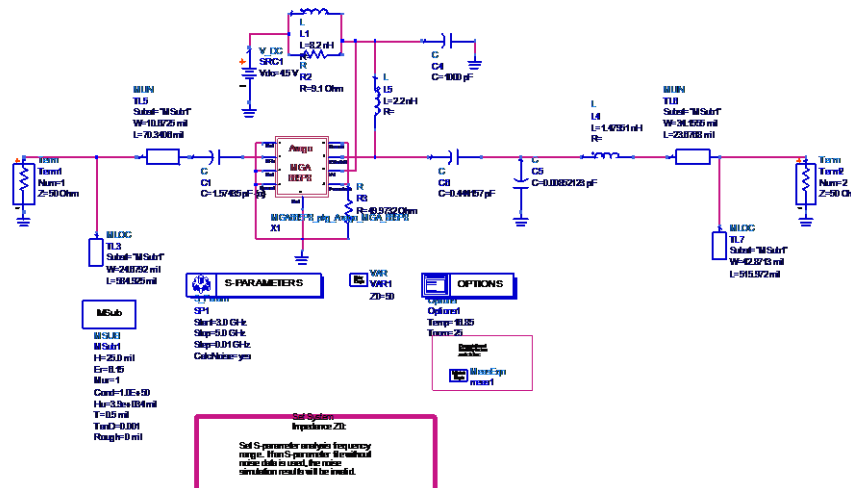


Fig. 9. Plot of associated power gain for  $V_d = 4.5V$

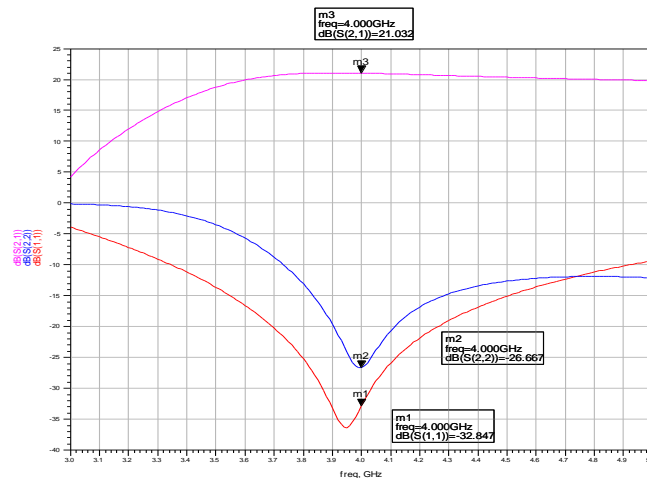


Fig. 10. Plots of gain (S21) and (S11) values for  $V_d = 4.5V$

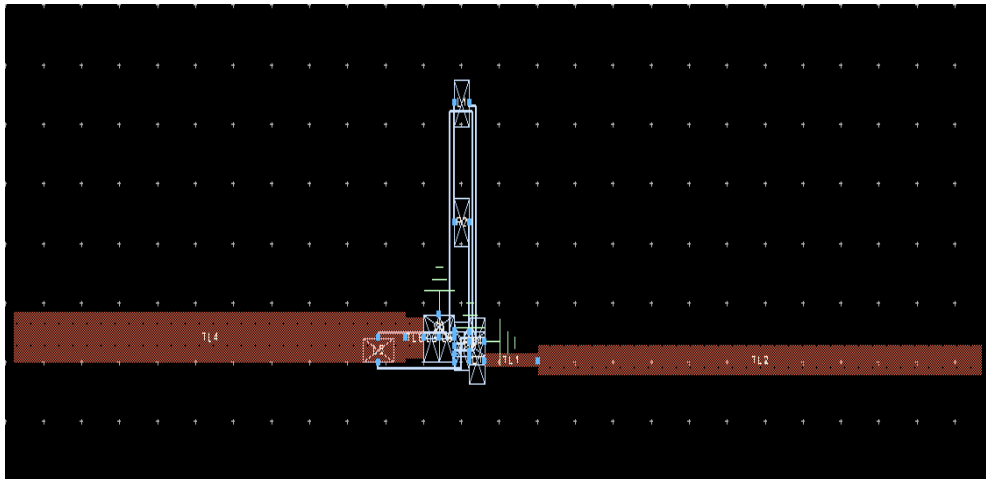


Fig. 11. Layout of the schematic circuit of proposed LNA shown in fig.7.

### 3. Conclusions

Wireless technology has been growing tremendously, with new applications reported almost every day. Besides the traditional applications in communication, such as radio and television, RF and microwaves are being used in cordless phones, cellular communication, local area networks (LANs), and personal communication systems (PCSs). Keyless door entry, radio frequency identification (RFID), monitoring of patients in a hospital or a nursing home, and cordless mice or keyboards for computers are some of the other areas where RF technology is being employed. While some of these applications have traditionally used infrared (IR) technology, radio frequency circuits are continuously taking over because of their

superior performance. The current rate of growth in RF technology is expected to continue in the foreseeable future. A single stage LNA with MGA-665P8 is designed and demonstrated with simulations in ADS package as well as tuning for the optimum noise figure and gain. The noise figure obtained for the LNA is 0.697dB, the gain is 21.032 dB. The design was tuned using optimization tools in ADS such that the final design (simulated with MGA-665P8) was improved in both gain and noise figure compared to the initial design (analytically and checked in simulations with S2P data). Optimization was performed mostly on the drain voltage bias point, and as well as on matching network. However no further improvement (regarding  $S_{11}$  and  $S_{21}$ ) was observed when optimization was performed on the matching network.

## References

- [1] S.Y. Liao, "Microwave devices and circuits." New Jersey: Prentice Hall, 3ed ed.,1990.
- [2] P.L.D. Abrie, "Design of RF and Microwave Amplifiers and Oscillators." USA: Artech House. 1999.
- [3] Available online at <http://www.avagotech.com/>
- [4] Available online at <http://www.agilent.com/>
- [5] Avago Technologies, "MGA-665P8 GaAs Enhancement-Mode PHEMT 0.5- 6GHz Low Noise Amplifier Data Sheet", [http://www.avagotech.com/products/rf\\_for\\_mobile\\_mmw/gps\\_lans\\_&\\_filters/mga-665p8/](http://www.avagotech.com/products/rf_for_mobile_mmw/gps_lans_&_filters/mga-665p8/)
- [6] mga-665p8/
- [7] Maxim, "Impedance Matching and the Smith Chart: The Fundamentals".[http://www.maxim-ic.com/appnotes.cfm/an\\_pk/742](http://www.maxim-ic.com/appnotes.cfm/an_pk/742),Nov 2008.
- [8] P.B. Kenington, "High-Linearity RF Amplifier Design." USA: Artech House Inc. 2000.
- [9] M. W. Medley, "Microwave And RF Circuits: Analysis, Synthesis And Design", USA: Artech House, 1993.
- [10] T. H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits". Cambridge: Cambridge University Press, 2nd ed., 2004.
- [11] 10 . G. Gonzalez, "Microwave Transistor Amplifiers: Analysis and Design". New Jersey: Prentice Hall, 2<sup>nd</sup> ed., 1996.
- [12] Ommic. "An Ultra Low Noise, High Linearity Amplifier". Microwave Journal.. 49 (4): 136, 2006.
- [13] Bahl, I. J., and P. Bhartia, "Microwave Solid State Circuit Design". New York: Wiley, 1988.
- [14] H. T. Friis, "Noise figure for radio receivers", Proc. of the IRE, 419-422, Jul. 1944.