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A Modified Topology of Asymmetrical 27-Levels Cascaded Multilevel Inverter

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Abstract*—Inverter design has changed greatly to fulfill the high expectations of technological developments, such as the operation of solar energy. This paper presents a new method to obtain an output voltage of 27 levels by using three asymmetric voltage sources and twelve power switches only instead of using fifty-two power switches and thirteen voltage sources, which leads to a reduction in costs and losses. The inverter was carried out by using the MATLAB Simulink program to install the inverter. THD% was calculated and the results obtained were compared with other studies.

Keywords— Cascaded H-Bridge, 27-levels, Multilevel Inverter.

I. INTRODUCTION

Multilevel inverters (MLI) are now regarded as one of the most important research and developments. Because of their numerous applications in high and medium voltage levels of activity [1]. Multi-level inverters have several advantages over a two-level inverter, including reducing THD%, reducing lower electromagnetic interference (EMI) and can operate in both high and medium power ratings [2]. In general, there are three main types of MLI are Cascaded H-Bridge (CHB), Flying Capacitor (FC) and Natural Point Clamped (NPC) [3].

CHB has a smaller number of components when compared with other two types. However, the main disadvantage of the cascaded hybrid bridge inverter is the number of DC sources and power switches increase with the output voltage level augmentation. Since each DC source needs a hybrid bridge cell and every cell consists of four switches [4]. To get 27 levels in output voltage waveform the CHB need 52 power switches and 13 DC supplies. The researchers in multilevel inverter have interested in reducing the number of switches and sources with to decrease the cost and losses. N.Prabaharan and K.Palanisamy in 2016 proposed a hybrid asymmetric MLI by using 5 DC supplies and 14 switches to get 27 level output voltage [5]. Saeid Deliri Khatoonabad and Kazem Varesi in 2020 introduce a novel construction of 27-level inverter by using 2 DC supplies, 13 unidirectional switches, 13 driver boards, 2 capacitors, and 1 diode [6].

This study proposes a new method of 27-level MLI uses 12 switches ,3 DC supplies and 16 diodes. MATLAB will be used to install the proposed inverter and measure the THD, and the results will be compared with other studies.

II. METHODOLOGY

A. Proposed Circuit Discription

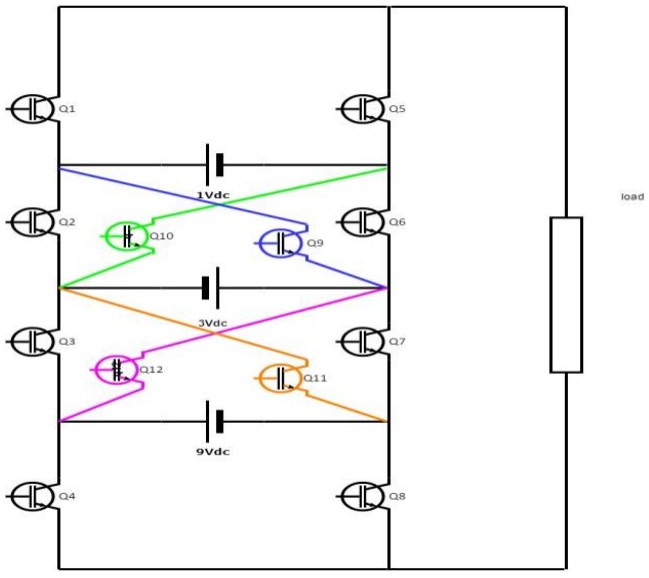


Figure 1 Proposed topology of modified cascaded H bridge inverter

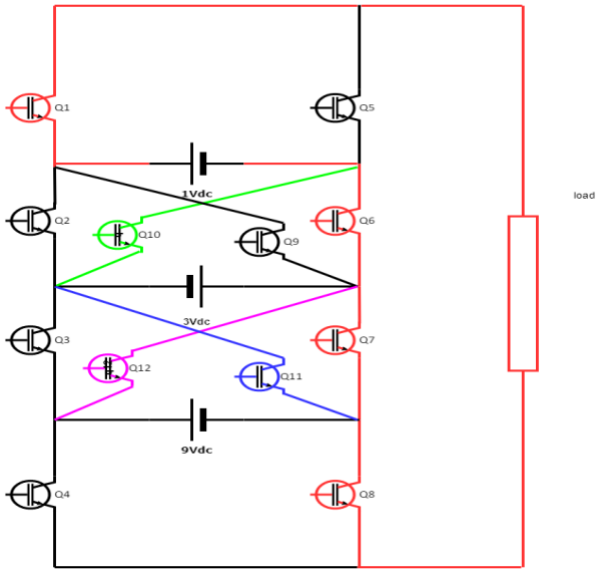
The Proposed inverter structure of a multi-level cascade inverter is seen in Fig. 1. It uses 12 switches and 3 DC supplies to create a 27-level output voltage waveform. In MCMLI, the DC voltage sources are not equal (V1 V2 and V3 in the ratio of 1:3:9, respectively). All switches

S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, and S12 cause changes in the output waveform's levels and polarity.

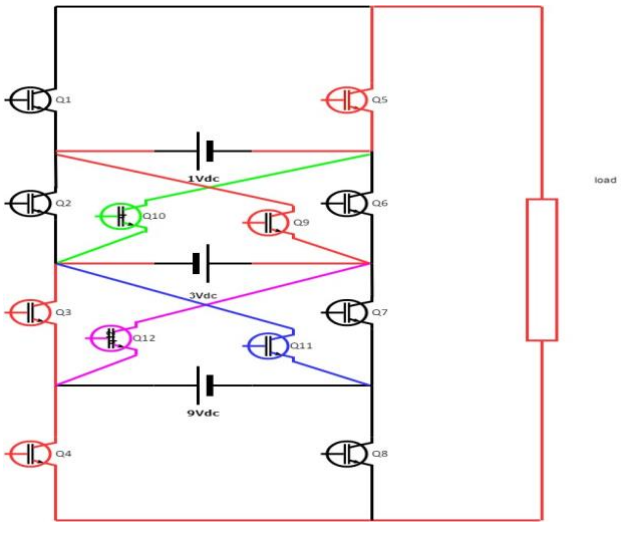
The circuit also consists of sixteen diodes to create paths and protect the X connection switches (S9, S10, S11, S10) from reverse current flow.

B. Intervals of the proposed inverter Operation

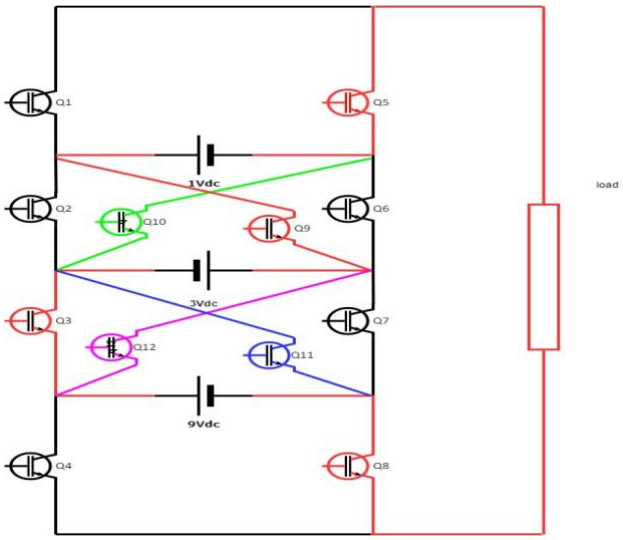
Fig.3 shows the sample of operation intervals of the proposed inverter. The Proposed inverter operational intervals are depicted in Fig. 3. Where (A, B, C, and D) represent the positive half-cycle operating intervals and (E, F, G, and H) represent the negative half-cycle operating intervals. The direction of the stream is represented by the red line at each interval. The inverter will operate at 27 distinct periods during one entire cycle.



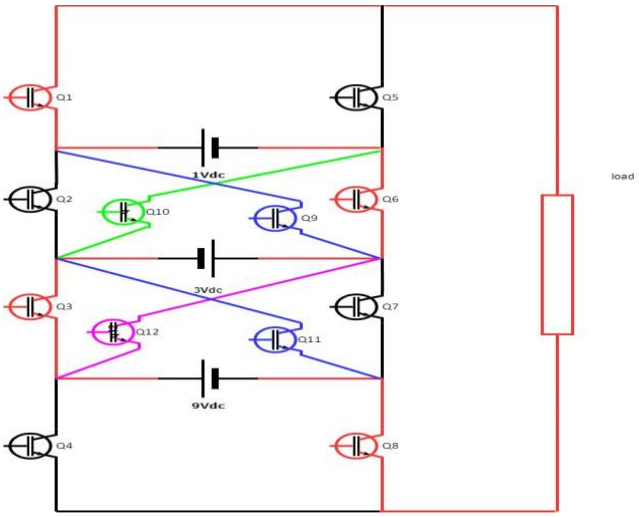
(A) V0=1V



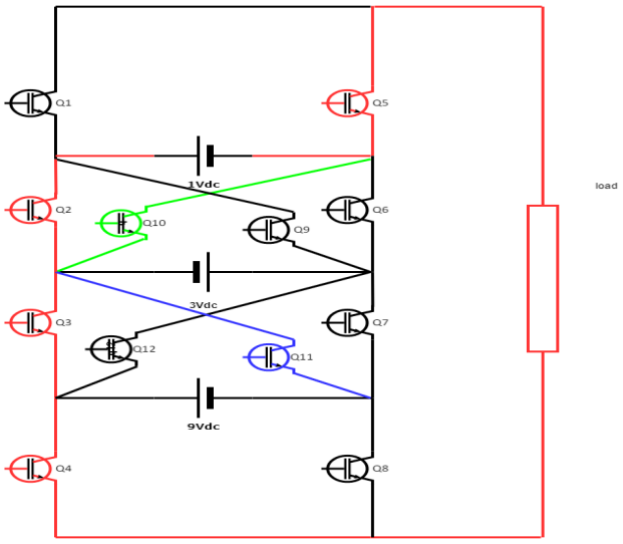
(B) V0=3V-1V=2V



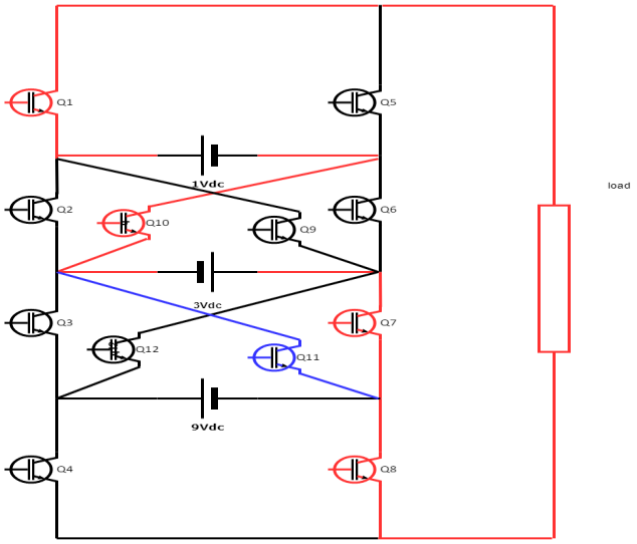
(C) V0=9V+3V-V1=11V



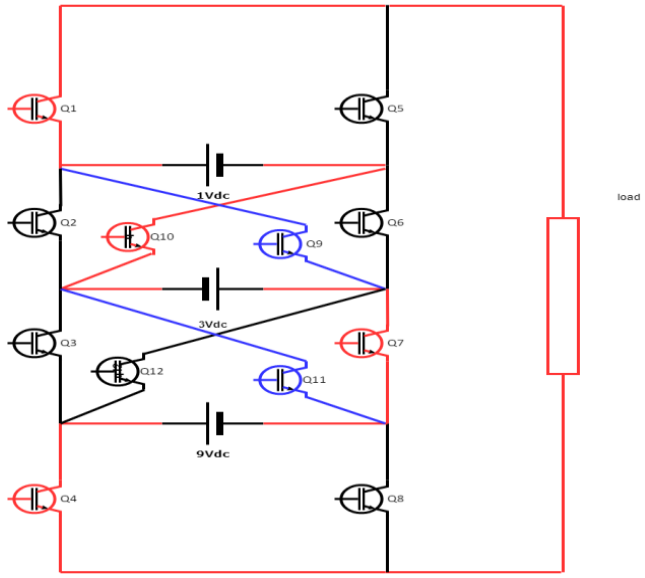
(D) V0=1V+3V+V1=13V



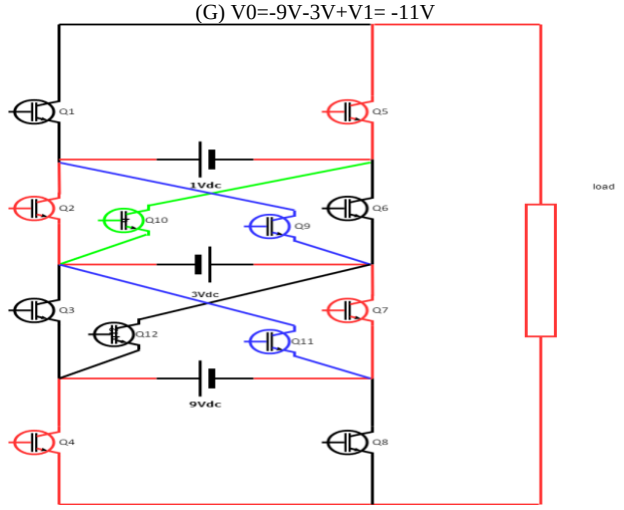
(E) V0= -1V



(F) V0=--3V+V= -2V



(G) V0=-9V-3V+V1= -11V



(H) V0=-1V-3V-V1= -13V

Figure 3 (A, B, C, D, E, F, G and H) Operating intervals of the Proposed inverter

Table 1 shows the switch states, with value 1 that the switch is turned on and 0 signaling that the switch is turned off. The first 13 intervals show the switching states for positive half cycle modes, whereas the following 13 intervals show the switching states for negative half cycle modes. fig 4 shows the control signals to the inverter switches.

TABLE 1. SWITCHING STATES OF INVERTER

		Switching sequence											
Interv	Output voltage	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12
1	Vo=0	0	0	0	0	0	0	0	0	0	0	0	0
2	Vo=1Vdc	1	0	0	0	0	1	1	1	0	0	0	0
3	Vo=2Vdc	0	0	1	1	1	0	0	0	1	0	0	0
4	Vo=3Vdc	0	0	1	1	1	1	0	0	0	0	0	0
5	Vo=4Vdc	1	0	1	1	0	1	0	0	0	0	0	0
6	Vo=5Vdc	0	1	0	0	1	0	0	1	0	0	0	1
7	Vo=6Vdc	1	1	0	0	0	0	0	1	0	0	0	1
8	Vo=7Vdc	1	0	0	0	0	0	0	1	0	1	0	1
9	Vo=8V	0	1	1	0	1	0	0	1	0	0	0	0
10	Vo=9Vdc	1	1	1	0	0	0	0	1	0	0	0	0
11	Vo=10Vdc	1	0	0	0	0	1	0	1	0	0	0	1
12	Vo=11Vdc	0	0	1	0	1	0	0	1	1	0	0	0
13	Vo=12Vdc	0	0	1	0	1	1	0	1	0	0	0	0
14	Vo=13Vdc	1	0	1	0	0	1	0	1	0	0	0	0
15	Vo=-1Vdc	0	1	1	1	1	0	0	0	0	0	0	0
16	Vo=-2Vdc	1	0	0	0	0	0	1	1	0	1	0	0
17	Vo=-3Vdc	1	1	0	0	0	0	1	1	0	0	0	0
18	Vo=-4Vdc	0	1	0	0	1	0	1	1	0	0	0	0
19	Vo=-5Vdc	1	0	0	1	0	1	0	0	0	0	1	0
20	Vo=-6Vdc	0	0	0	1	1	1	0	0	0	0	1	0
21	Vo=-7Vdc	0	0	0	1	1	0	0	0	1	0	1	0
22	Vo=-8Vdc	1	0	0	1	0	1	1	0	0	0	0	0
23	Vo=-9Vdc	0	0	0	1	1	1	1	0	0	0	0	0
24	Vo=-10Vdc	0	1	0	1	1	0	0	0	0	0	1	0
25	Vo=-11Vdc	1	0	0	1	0	0	1	0	0	1	0	0
26	Vo=-12Vdc	1	1	0	1	0	0	1	0	0	0	0	0
27	Vo=-13Vdc	0	1	0	1	1	0	1	0	0	0	0	0

III. .SIMULATION RESULTS

The simulation model presented in Fig 4 is created in Matlab-Simulink software to evaluate the execution of the proposed inverter. At a fundamental frequency of 50Hz, Proposed inverter is simulated. To produce a ternary source arrangement with a maximum output of 260volt, the DC sources are set to V1=20volt, V2=60volt, V3=180volt, and the resistive load is set to 100ohm. The major switches in this circuit were BJT. PWM with selective harmonic elimination is used to

manage the output voltage. Figure 3 depicts the control signal for switches all switches are shown

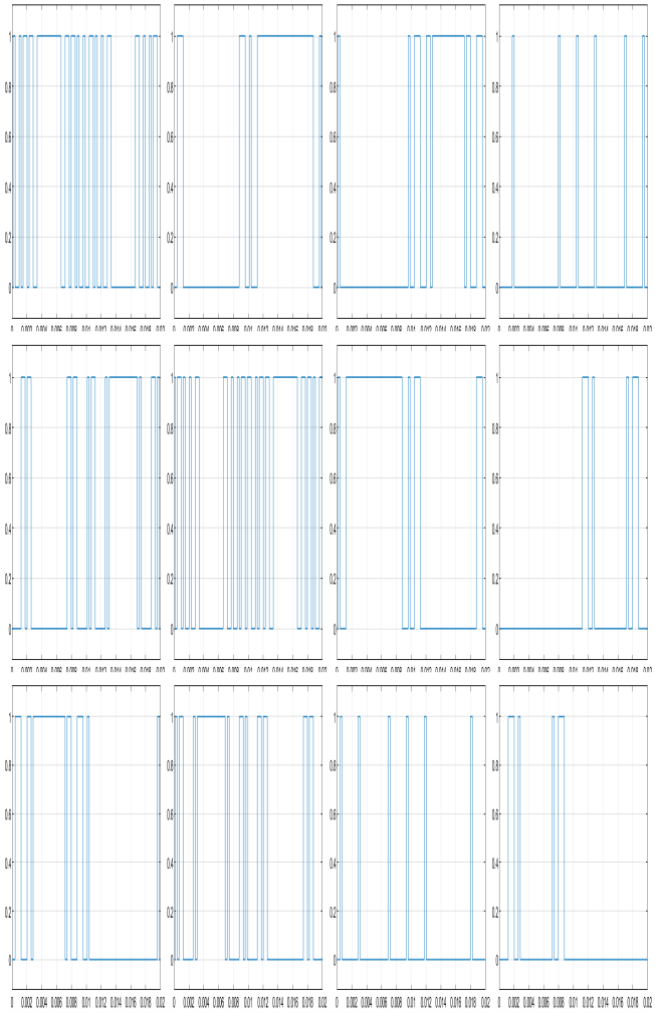


Figure 4 control signals to the inverter switches

Figure.5 shows the circuit of MCMLI as presented in simulation process in MATLAB program which is consisting of 12 switches and 16 diodes, 3 DC sources with 3 subsystems for the control circuit. The subsystem consists of logic gates AND, OR, and NOT, and pulse generators. The switching sequence for different step size is shown in table 2.

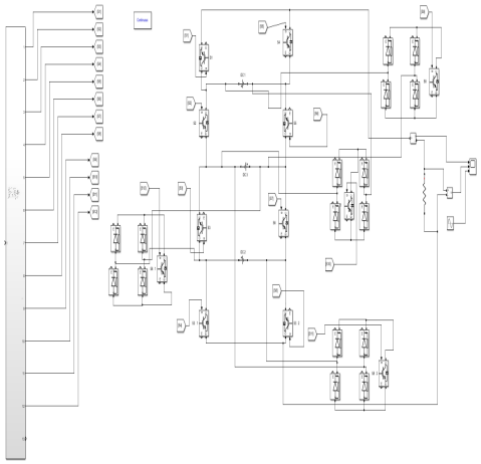


Figure 5 simulation diagram of the Proposed inverter

Table 2 shows the switching states and angles of all duration times for all cases.

TABLE 2. ANGLES OF ALL DURATION TIMES

Intervals	Output voltage	Case2 360/76=4.74	Case3 360/80=4.5	Intervals	Output voltage	Case2 360/76=4.74	Case3 360/80=4.5
1	Vo=0	0 to 2.36	0 to 2.26	27	Vo=0	177.596 to 182.332	177.75 to 182.25
2	Vo=1V	2.36 to 7.1	2.25 to 6.75	28	Vo=-1V	182.332 to 187.068	182.25 to 186.75
3	Vo=2V	7.1 to 11.8	6.75 to 11.25	28	Vo=-2V	187.068 to 191.804	186.75 to 191.25
4	Vo=3V	11.8 to 16.572	11.25 to15.75	29	Vo=-3V	191.804 to 196.54	191.25 to 195.75
5	Vo=4V	16.572 to 21.308	15.75 to 20.25	30	Vo=-4V	196.54 to 201.276	195.75 to 200.25
6	Vo=5V	21.308 to 26.044	20.25 to 24.75	31	Vo=-5V	201.276 to 206.012	200.25 to 204.75
7	Vo=6V	26.044 to 30.78	24.75 to 29.25	32	Vo=-6V	206.012 to 210.748	204.75 to 209.25
8	Vo=7V	30.78 to 35.516	29.25 to 33.75	33	Vo=-7V	210.748 to 215.484	209.25 to 213.75
9	Vo=8V	35.516 to 40.252	33.75 to 38.25	34	Vo=-8V	215.484 to 220.22	213.75 to 218.25
10	Vo=9V	40.252 to 44.988	38.25 to 42.75	35	Vo=-9V	220.22 to 224.956	218.25 to 222.75
11	Vo=10V	44.988 to 49.724	42.75 to 47.25	36	Vo=-10V	224.956 to 229.692	222.75 to 227.25
12	Vo=11V	49.724 to 54.46	47.25 to 51.75	37	Vo=-11V	229.692 to 234.428	227.25 to 231.75
13	Vo=12V	54.46 to 59.196	51.75 to 56.25	38	Vo=-12V	234.428 to 239.164	231.75 to 236.25
14	Vo=13V	59.196 to 120.764	56.25 to 123.75	39	Vo=-13V	239.164 to 300.732	236.25 to 303.75
15	Vo=12V	120.764 to 125.5	123.75 to 128.25	40	Vo=-12V	300.732 to 305.468	303.75 to 308.25
16	Vo=11V	125.5 to 130.236	128.25 to 132.75	41	Vo=-11V	305.468 to 310.204	308.25 to 312.75
17	Vo=10V	130.236 to 134.972	132.75 to 137.25	42	Vo=-10V	310.204 to 314.94	312.75 to 317.25
18	Vo=9V	134.972 to 139.708	137.25 to 141.75	43	Vo=-9V	314.94 to 319.676	317.25 to 321.75
19	Vo=8V	139.708 to 144.444	141.75 to 146.25	44	Vo=-8V	319.676 to 324.412	321.75 to 326.25
20	Vo=7V	144.444 to 149.18	146.25 to 150.75	45	Vo=-7V	324.412 to 329.148	326.25 to 330.75
21	Vo=6V	149.18 to 153.916	150.75 to 155.25	46	Vo=-6V	329.148 to 333.884	330.75 to 335.25
22	Vo=5V	153.916 to 158.652	155.25 to 159.75	47	Vo=-5V	333.884 to 338.62	335.25 to 339.75
23	Vo=4V	158.652 to 163.388	159.75 to 164.25	48	Vo=-4V	338.62 to 343.356	339.75 to 344.25
24	Vo=3V	163.388 to 168.124	164.25 to 168.75	49	Vo=-3V	343.356 to 348.092	344.25 to 348.75
25	Vo=2V	168.124 to 172.86	168.75 to 173.25	50	Vo=-2V	348.092 to 352.828	348.75 to 353.25
26	Vo=1V	172.86 to 177.596	173.25 to 177.75	51	Vo=-1V	352.828 to 357.564	353.25 to 357.75
27	Vo=0	177.596 to 182.332	177.75 to 182.25	52	Vo=-0V	357.564 to 360	357.75 to 360

Case 1: Simulation with resistive load:

In this case, using unequal space control as well but only the peak step is bigger than other steps by thirteen

times, the number of switching pulses is 74 pulses. In figure 6 the waveform of the current and voltage are shown.

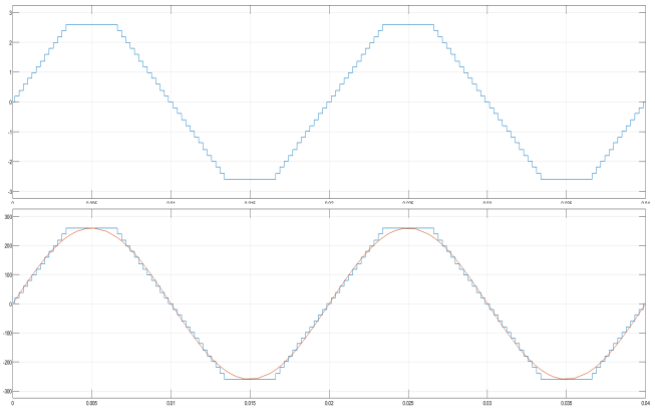


Figure 6 current and voltage wave forms of case 1

Figure 7, shows the result of THD and harmonic orders, the biggest harmonic order is the fifth-order after that the third and seventh orders then around the switching frequency harmonics before and after the switching frequency. These are the seventy-third and seventy-fifth orders.

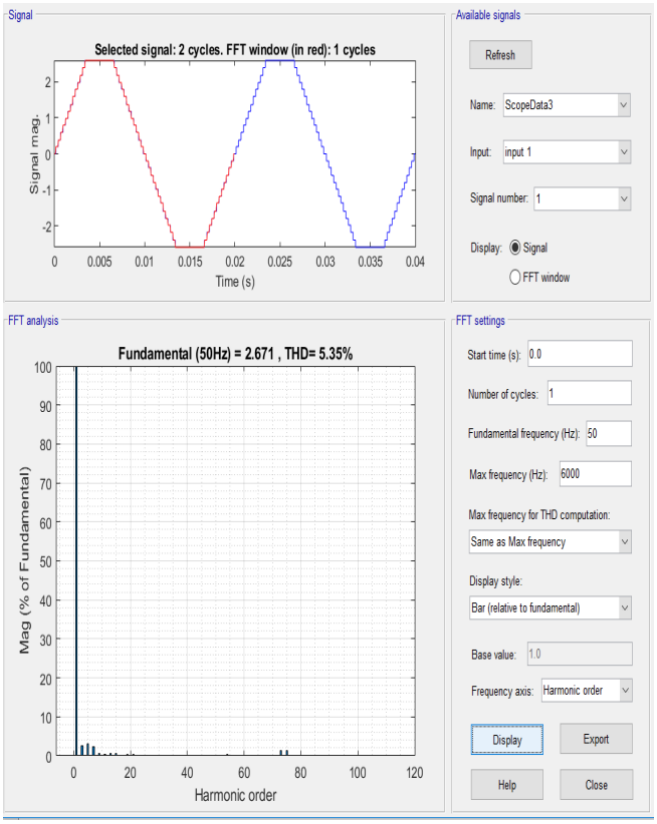


Figure 7 current and voltage wave form and the THD

Case 2: Simulation with inductive load:

In this case use same control of case 1 with, R=80ohm and XL=20ohm, (L=64 mH) is used. In this case, using unequal space control, similar to case 1 in the previous section whose the peak step is bigger than other steps by fifteen times. Figure 8 shows the waveform of the voltage and current and the effect of inductive loading on the current waveform is quite clear.

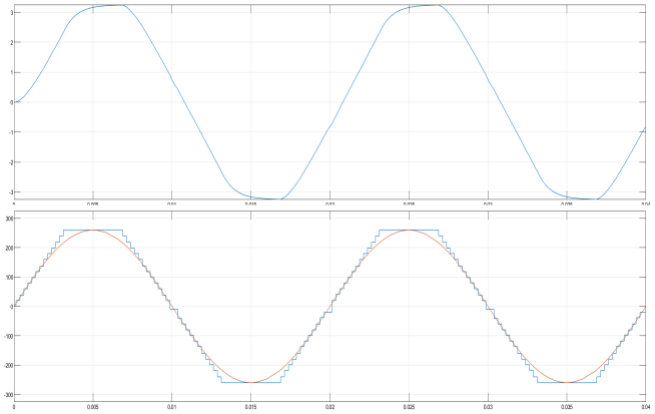


Figure 8 current and voltage wave forms with inductive load for case 2

Figure 9, shows the result of THD and harmonic orders, the biggest harmonics order are the third, fifth, seventh, ninth, and eleventh orders. This is the effect of inductive because it is filtering out the higher-order harmonics of the current waveform.

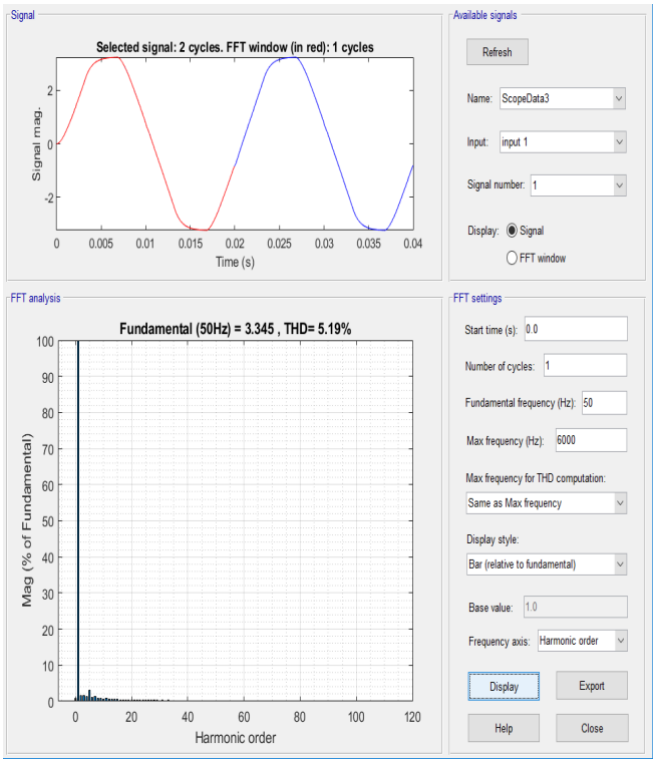


Figure 9 current wave form and the THD for case2 with inductive load

Figure 10, shows the result of THD and harmonic orders, the biggest harmonic order is the fifth-order after that the switching frequency effect for the harmonic orders and it generates two harmonics before and after the switching

frequency. These are the seventy-ninth and eighty-first order, and finally the seventh-order has big value.

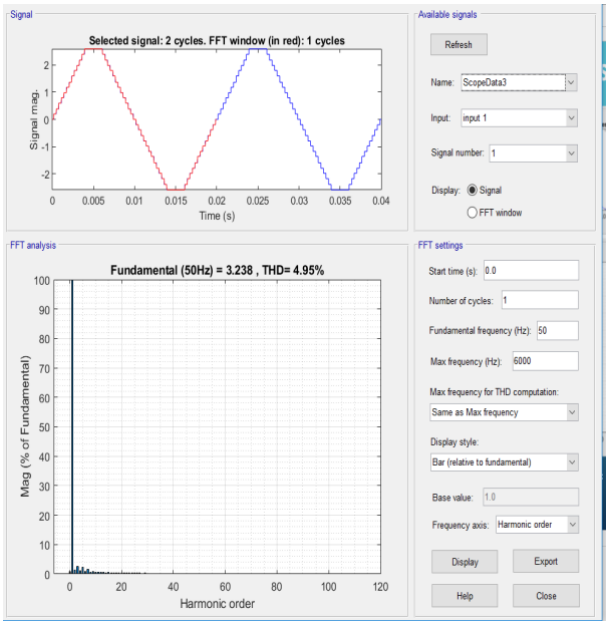


Figure 10 current wave form and the THD for case2 with inductive load

Table 3 shows comparison of results obtained in this paper with other study results in terms of harmonic distortion.

TABLE 3. THD% COMPARISON

References	THD%
This study	4.95%
[5]	4.28%
[6]	1.93%
[7]	Different value depends on PWM type (from 4.41% to 5.73%)

IV. CONCLUSION

In this study, a novel asymmetric cascaded multilevel inverter was presented to create 27-level output waveforms. The Technological control of this circuit is PWM (selective harmonic elimination). In comparison to alternative topologies, a single phase 27 level reduced switches and DC sources. The suggested MLI has just 12 switches and three DC sources to provide a 27-level output voltage. The inductive loading effect in filtering out the high order harmonics components is more noticeable in current waveforms but the voltage waveform is still unaffected. The simulation results reveal that the THD=4.95% for the proposed network's output voltages which is low when compared to other MLI networks and no filter is used.

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