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Investigating Performance Parameters of Class E Power Amplifier with Shunt Capacitance Configuration at Lower Microwave Frequency Band

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Abstract: Class E power amplifier circuit consists mainly of a transistor operates as a switch, load network and series LC filter tuned to fundamental frequency.
There is different configurations to realize class E power amplifier circuit according to the load network such as: shunt capacitance configuration, shunt inductance configuration and parallel circuit configuration.

In this paper the performance parameters (such as: PAE, overall efficiency, drain efficiency, gain, drain voltage and current waveforms) of class E power amplifier with shunt capacitance configuration at frequencies [0.25, 0.5, 0.75 and 1 GHz] are observed

1 INTRODUCTION

Power amplifier is an important part of radio communication devices in both transmitter and receiver sides, they have wide spread applications such as: mobile phones, base stations, radars, space-based systems.

The need for high efficiency power amplifiers is increased because higher efficiency means less power dissipation which leads to less required DC power, long battery life time, small battery size also, less power dissipation (means less heat) so less heat sink is required. All of that reduces as a result the cost and the physical size of the power amplifier

Power amplifiers are categorized into two broader categories: transconductance amplifiers (class A, class B, class AB, class C) and switching mode power amplifiers (class D, class E, class F) based on the property that either the power amplifier is linear or nonlinear. [1]

Transconductance amplifiers are linear amplifiers, class A is the most linear then class B, then class AB and least linear class C, the linearity degrades as a cost of efficiency increase. Switching mode power amplifiers can achieve a much higher efficiency than the transconductance amplifiers.

Class E power amplifier is one of the switching mode power amplifiers that can achieve theoretical efficiency of 100%, and relatively easy to design with small size and light weight.

2 CLASS E POWER AMPLIFIER

Theoretically Class E power amplifier has maximum efficiency of 100%, the main components of the circuit of Class E PA are: a transistor working as switch and a passive load network designed to minimize drain (collector) voltage and current waveforms overlapping which minimize power dissipation in the transistor to achieve maximum efficiency.

To simplify the analysis of a Class-E power amplifier, the following several assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off resistance, and its switching action is instantaneous and lossless.
- The total shunt capacitance is independent of the collector and is assumed linear.
- The RF choke allows only a constant dc current and has no resistance.
- The loaded quality ($Q_L = \omega L_o/R = 1/\omega C_o R$) factor of the series resonant L_oC_o circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except only in the load *R* (ideal passive components and the transistor acts as an ideal switch).
- For an optimum operation mode, a 50% duty cycle is used.[1]

Raab [4] defined optimum class E power amplifier which satisfies all the following conditions:

1. The peak drain voltage and current do not exist simultaneously.
2. At the end of the rise section of the drain current waveform, it must decrease to zero before the rise section of the voltage waveform can start. In other words, the current reaches zero at the end of the ON interval right before the switch is turned off. The beginning of the rise section of the voltage waveform should be delayed until after the switch is turned off.
3. The slope of the current waveform at the end of its rise section must be zero to avoid power dissipation due to the existence of both current and voltage. The similar conditions apply to the drain voltage waveform at the end of its rise section.

4. It must return to zero at the end of the switch OFF interval (right before the switch is turned on) before the rise of the current waveform can start.
The starting point of the rise section of the current waveform should be postponed until after the transistor is turned on.
5. Its slope is zero at that moment to avoid power dissipation due to the simultaneous imposition of current and voltage.

All the above conditions are meant to eliminate the power dissipation of the transistor as much as possible during the class E operation to increase the efficiency. [3]

The load network of class E power amplifier has several configurations such as shunt capacitance, parallel circuit and shunt inductance.

2.1 Class E with shunt capacitance

The simplified equivalent circuit of class E power amplifier with a shunt capacitance is shown in Fig. 1 where the load network consists of a capacitor *C* shunting the transistor, a series inductor *L*, a series fundamentally tuned filter L_oC_o and a load resistor *R*. In a common case, a shunt capacitor *C* can represent the intrinsic device output capacitor and external circuit capacitor added by the load network.

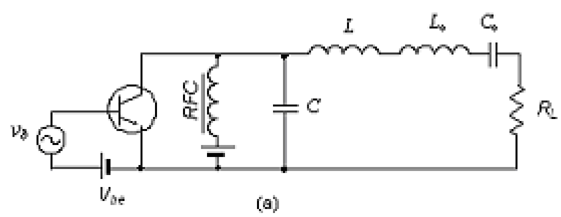

Figure 1: Class E Power Amplifier with Shunt Capacitance

Numerous literatures have presented some mathmatical analysis of the class E power amplifier with shunt capacitance, most of which are tedious. The most widely used design equations for optimum circuit parameters are provided in seversl sources [1],[3],[4] and are listed as follows:

$$R = 0.5768 \frac{V^2_{CC}}{P_{out}} \quad (1)$$

$$L = 1.1525 \frac{R}{\omega} \quad (2)$$

$$C = \frac{1}{5.4466\omega.} \quad (3)$$

Where:

R: Optimum value of load resistance.
L: Optimum value of series inductance.
C: Optimum value of shunt capacitance.
ω : Operating frequency in rad..
P_{out}: Desired output power.
Vcc: DC collector supply voltage.

Fig. 2 shows the normalized (a) collector voltage and (b) collector current waveforms for an idealized optimum Class E with shunt capacitance. [1]

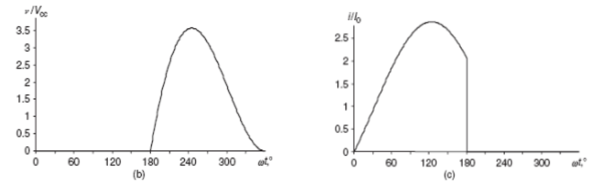

Figure 2:(a) Normalized collector voltage waveform.
(b) Normalized collector current waveform.

2.2 Class E with Parallel Circuit

The theoretical analysis of a switched-mode parallel-circuit Class-E power amplifier using a series filter with the calculation of the voltage and current waveforms and some graphical results are found in [1].

The basic circuit of a switched-mode parallel-circuit Class-E power amplifier is shown in Fig. 3 a. The load network consists of a finite dc-feed inductor *L*, a shunt capacitor *C*, a series L_oC_o -resonant circuit tuned to the fundamental frequency, and a load resistor *R*.

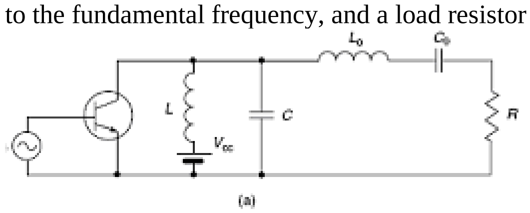

Figure 3: Class E power amplifier with parallel circuit

Normalized collector current and collector voltage waveforms for an idealized optimum parallel-circuit Class-E operation is the same as shown in Fig. 2. From collector voltage and current waveforms, it follows that, similar to other Class-E subclasses, there is no nonzero voltage and current simultaneously. When this happens, no power loss occurs and an idealized collector efficiency of 100% is achieved.

The design equations for optimum load resistance *R*, parallel inductance *L*, and parallel capacitance *C* are as follows:

$$R = 1.365\frac{V^2_{CC}}{P_{out}} \quad (4)$$

$$L = 0.732\ \frac{R}{\omega} \quad (5)$$

$$C = \frac{0.685}{\omega R} \quad (6)$$

Where:

R: Optimum value of load resistance.
L: Optimum value of shunt inductance.
C: Optimum value of shunt capacitance.
ω : Operating frequency in rad..
P_{out}: Desired output power.
Vcc: DC collector supply voltage.

2.3 Class E with Shunt Inductance

An alternate approach to the design of the Class E power amplifier with an efficiency of 100 percent under idealized operation conditions is to use shunt inductance. Such a Class E power amplifier is similar to the Class E power amplifier with shunt capacitance but in this case the storage element is inductive. The basic circuit of a Class E power amplifier with shunt inductance is shown in Fig. 4

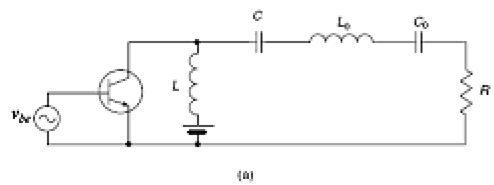

Figure 4: ClassE Power Amplifier with
Shunt Inductance Circuit

The loading circuit consists of the inductance *L* connected in parallel to the output of the transistor terminals, the series capacitance *C*, the series filtering circuit L_oC_o tuned on the fundamental frequency and load resistance *R*.

The optimum values of the loading network parameters are given as follows [2]:

$$R = 0.05844\frac{V^2_{CC}}{P_{out}} \quad (7)$$

$$L = 5.4466\ \frac{R}{\omega} \quad (8)$$

$$C = \frac{0.2329}{\omega R} \quad (9)$$

Where:

R: Optimum value of load resistance.
L: Optimum value of shunt inductance.
C: Optimum value of shunt capacitance.
ω : Operating frequency in rad..
P_{out}: Desired output power.
Vcc: DC collector supply voltage.

3 DESIGN AND SIMULATION

Design and simulation of class E power amplifier with shunt capacitance configuration at operating frequencies from 0.25 GHz to 1 GHz in steps of 0.25 GHz with following operating conditions:

P_{out}	Output power	500 mW
P_{in}	Input power	10 mW
Q_L	Loaded quality factor	10
V_{DD}	Drain DC supply voltage	2.6 V
V_{GG}	Gate voltage	-2 V

is performed using ADS (Advanced Design System) in order to investigate and observe the performance parameters (PAE, overall efficiency, power gain, DC power, output power …etc) of this configuration at each operating frequency.

The elements values of the load network are calculated using equations (1-3) as start values, using ADS these values are optimized and the optimum performance parameters are evaluated.

Fig 5. shows ADS simulation of class E power amplifier with shunt capacitance at 0.25 GHz.

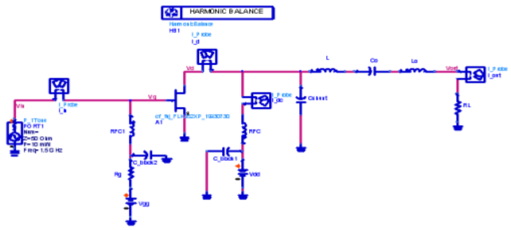

Figure 5: ADS class E PA circuit with shunt capacitance configuration.

The drain voltage and current waveforms, PAE, overall efficiency, drain efficiency and gain in dB of class E power amplifier with shunt capacitance configuration at frequency 0.25 GHz are shown in Figures. (6-10) respectively.

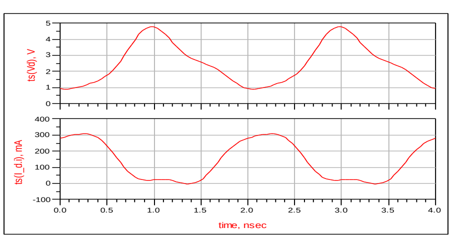

Figure 6: Drain voltage and current for class E PA with shunt capacitance configuration at 0.25 GHz

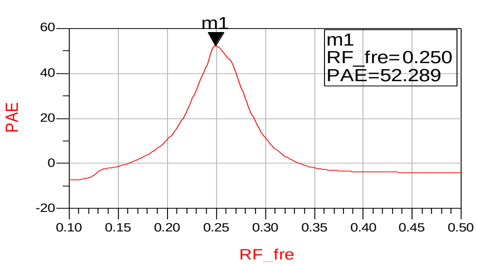

Figure 7: Power added efficiency PAE of class E PA with shunt capacitance configuration at 0.25 GHz.

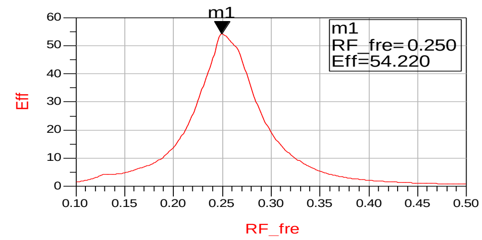

Figure 8: Overall efficiency η_{all} of class E PA with shunt capacitance at frequency 0.25GHz.

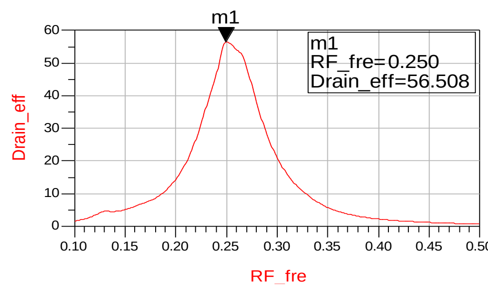

Figure 9: Drain efficiency η_{drain} of class E PA with shunt capacitance at frequency 0.25GHz

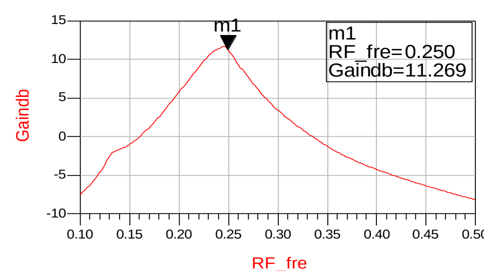

Figure 10: Gain in dB of Class E PA Circuit with Shunt Capacitance Configuration at 0.250 GHz.

Same above work is done at frequencies (0.5 GHz, 0.75 GHz, and 1 GHz) and the results are tabulated in table 1 and shown graphically in Figs. (11-14) respectively.

Table 1: PAE, overall efficiency, drain efficiency and gain in dB for shunt capacitance configuration at frequencies (0.25 GHz, 0.5 GHz, 0.75 GHz and 1 GHz)

f (GHz)	**PAE %**	**η_{all} %**	**η_{drain} %**	**Gain (dB)**

0.250	52.289	54.220	56.508	11.269
0.500	47.868	50.021	52.176	10.831
0.750	45.063	47.398	49.502	10.474
1	43.589	45.953	47.963	10.400

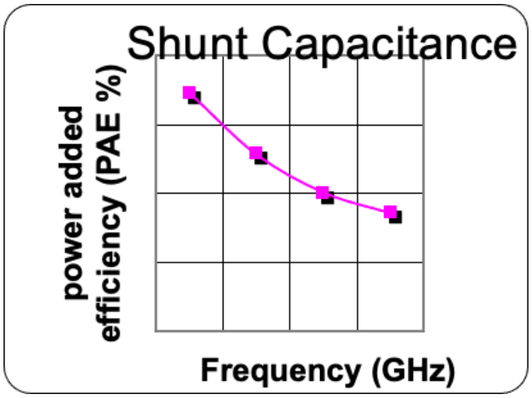

Figure 11: Power Added Efficiency PAE of Class E PA with shunt capacitance circuit configuration at frequencies: 0.250, 0.500, 0.750 and 1 GHz.

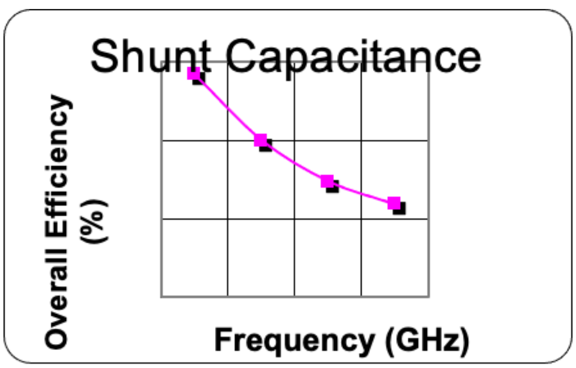

Figure 12: overall Efficiency of Class E PA With shunt capacitance Circuit Configuration at frequencies: 0.250, 0.500, 0.750 and 1 GHz.

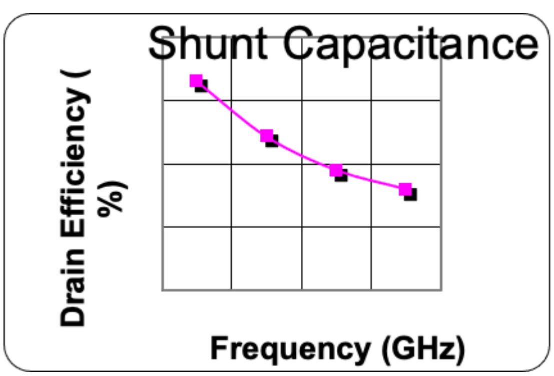

Figure 13: Drain efficiency of Class E PA With shunt capacitance Circuit Configuration at frequencies: 0.250, 0.500, 0.750 and 1 GHz.

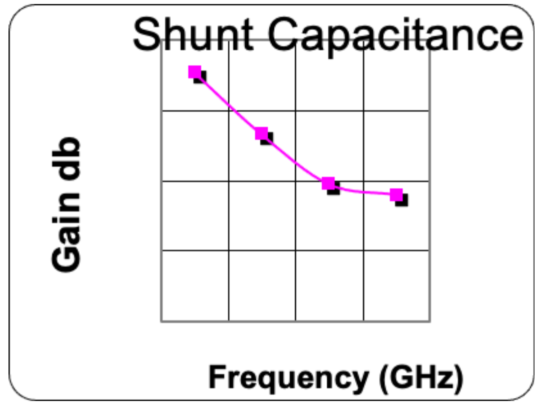

Figure 14: Gain in dB of Class E PA With shunt capacitance Circuit Configuration at frequencies: 0.250, 0.500, 0.750 and 1 GHz.

4 CONCLUSIONS

Class E power amplifier with shunt capacitance configuration circuit is designed at each frequency of the frequencies (0.25, 0.5, 0.75, 1 GHz) and simulated using ADS and the performance parameters of the circuit at each frequency is observed and it is noted that:

“Class E power amplifier with shunt capacitance circuit gives better performance (PAE, overall efficiency, drain efficiency, and power gain) at frequency 0.25 GHz then it degrades as the frequency of operation increases and as expected, this is caused by the parasitic components in the transistor (such as stray capacitance and bond wire inductances) and passive load network elements (such as electrical series resistance of capacitors and inductors) , the effect of these parasitic components increases as frequency of operation increase, this increase of these parasitic components causes increase of power dissipation which causes decrease in efficiency and gain and the overall performance of the amplifier”.

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